REMARKS/ARGUMENTS

Favorable reconsideration of this application as presently amended and in light of the following discussion is respectfully requested.

Claims 1, 4-7, 10-13 and 15-25 are presently active in this case. Claims 1, 7, 13, and 16 having been amended, Claims 2, 8 and 14 canceled and Claims 20-25 added by the present Amendment, Claims 3, 9 and 14 having been previously canceled.

In the outstanding Official Action Claims 1, 2, 4, 7, 8, 10, 13, 15 and 16 were rejected under 35 USC §102(b) as being anticipated by Stolmeijer et al (US 5,742,090) (hereing after called "Stolmeijer") and Claims 5, 6, 11, 12 and 17-19 were rejected under 35 USC §103(a) as being unpatentable over Stolmeijer.

First, new Claims 20-25 are submitted herewith to define Applicants' invention in varying scope. Examination on the merits of Claims 20-25 is respectfully requested.

In light of the several renewed grounds for rejection, Claim 1 has been amended to accentuate what are believed to be clearly distinguishing features over Stolmeijer, and to that end, more clearly patentably define over this reference. Accordingly, amended Claim 1 recites first and second conductive type layers configured as first and second electrodes of a capacitor, and a well area, i.e., the construction of a capacitor. The claimed deice further includes a low-resistance area formed at the base portion of the well area and having a resistance lower than that of the well area. Therefore, even if the space is broadened between the first conductivity type semiconductor layer and the second conductivity type semiconductor layer in order to reduce the capacitance of the line connected to a capacitor, it is possible to keep the well resistance low. In addition, the low-resistance area is not in contact with the depletion layer of the junction portion between the first conductivity type semiconductor layer and the well area, but in contact with the element isolation areas.

Therefore, the resistance can be lowered at portions under the element isolation areas, which results in the advantages that it is possible to keep the well resistance low, even if the space is broadened between the element areas, and thus to suppress thermal noise.

In contrast, in FIG. 5 of Stolmeijer, high-dopant regions 81, 82 are formed in a well region 120, and high-dopant regions 83, 84 are formed in a well region 220. However, as shown in FIG. 4, the well regions 81 to 84 are formed on the periphery of trenches 71, 72, 74 and 75, and therefore, the well regions are provided to suppress the latch-up phenomenon of a transistor. For this reason, Stolmeijer does not mention an electrode of a capacitor. The outstanding Office Action indicates in regard to claim 16 that Stolmeijer discloses a capacitor having plates 83, 30, and another capacitor having plates 81, 30. However, region 30 is the source/drain region of a MOS transistor, and region 81 is a region for suppressing the latch-up phenomenon of the MOS transistor. Therefore, Stolmeijer does not suggest that regions 81, 30 function as electrodes of a capacitor and clearly includes no teachings per se directed to a capacitor.

Moreover, Stolmeijer most certainly does not show the positions of field regions 120, 210 clearly. That is to say, the low-resistance area of amended Claim 1 is defined in contact not with the depletion layer of the junction portion between the semiconductor layers and the well area, but with the element isolation areas, while Stolmeijer does not show to what extent field regions 120, 210 are formed. Stolmeijer is silent in regard to the relationship between a low resistance region formed in a well and depletion layers formed by capacitor electrodes in the well.

Thus, insofar as Stolmeijer is directed to the structure of transistors and not of capacitors formed in a well, and includes no teachings in regard to low resistance regions formed in a well in regard to capacitor electrodes or depletion regions produced by capacitor

electrodes in the well, it is respectfully submitted that Stolmeijer clearly does not teach each feature of amended Claim 1 and thus cannot provide a basis for an anticipation rejection under 35 USC §102. Furthermore, the deficiencies of Stolmeijer are of such significance that absent hindsight, there is clearly insufficient basis under 35 USC §103 to reject Claim 1. Accordingly, it is respectfully submitted that Claim 1 patentably defines over Stolmeijer and is in condition for allowance.

Claim 7 recites a first semiconductor layer formed in a first well area functions as a node for applying a potential to the first well area, and a first low-resistance area is in contact with element isolation areas. Accordingly, the potential can be applied to the first well area without loss, and it is possible to implement a high-gain amplifier.

In contrast, in FIG. 5 of Stolmeijer a structure corresponding to the first semiconductor layer or first low-resistance area of Claim 7 is neither shown nor suggested. Therefore, claim 7 cannot be anticipated by Stolmeijer, and it is respectfully submitted that Claim 7 also patentably distinguishes over Stolmeijer.

Amended Claim 13 recites a base layer of a bipolar transistor is formed on a first well area serving as a first electrode of the bipolar transistor, and a second electrode of the bipolar transistor is formed on the base layer. Further, a first low-resistance area is formed at a bottom portion of the first well area. The first low-resistance area is in contact not with the junction portion of the bipolar transistor, but with element isolation areas. Therefore, it is possible to suppress power loss of the bipolar transistor and to implement a high-gain amplifier. Therefore, it is respectfully submitted that Claim 13 cannot be anticipated by Stolmeijer, and that Claim 13 likewise patentably distinguishes over Stolmeijer.

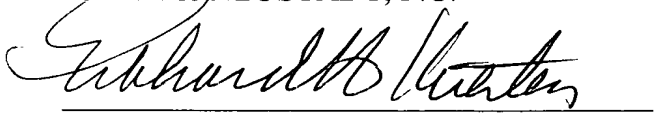
Amended claim 16 recites an analog circuit formed in a first well area, and a digital circuit formed in a second well area. A low-resistance area is provided in the first well area

excluding the second well area. In contrast, Stolmeijer merely discloses a MOS transistor. The outstanding Office Action states that Stolmeijer discloses a MOS transistor, a bipolar transistor and a capacitor having plates 81, 30. However, region 30 is the source/drain region of the MOS transistor, and region 81 is a region for suppressing the latch-up phenomenon. Therefore, Stolmeijer does not suggest that regions 81, 30 function as electrodes of a capacitor. Further, Stolmeijer merely disclose a MOS transistor, but does not suggest a bipolar transistor or an analog circuit. Moreover, according to Stolmeijer field region 120 is formed in well region 130, and field region 220 is formed in well region 230. Accordingly, Stolmeijer does not disclose that a low-resistance area is formed only in a well region in which an analog circuit is formed. Therefore, it is respectfully submitted that Claim 16 cannot be anticipated by Stolmeijer and is also patentably distinguishing over Stolmeijer.

Consequently, in view of the present amendment, independent Claims 1, 7 and 16, as well as the remaining claims dependent therefrom, are believed to be patentably distinguishing over the applied prior art and in condition for allowance. An early and favorable action to that effect is respectfully requested.

Respectfully submitted,

OBLON, SPIVAK, McCLELLAND,
MAIER & NEUSTADT, P.C.



Eckhard H. Kuesters
Attorney of Record
Registration No. 28,870

Customer Number
22850

Tel: (703) 413-3000
Fax: (703) 413 -2220
(OSMMN 08/03)